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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,162	01/11/2002	Shahram Mostafazadeh	NSC1P225R	3102

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BEYER WEAVER & THOMAS LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AHC

Office Action Summary	Application No.	Applicant(s)	
	10/044,162	MOSTAFAZADEH ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Reissue Applications

1. Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. 6,117,710 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Claim Objections

2. Claims 2-3 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitations of these two claims are parts of the newly added limitations in claim 1.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. US 5,252,855 in combination with Melton et al. US 5,844,315 and Djennas et al. US 5,474,958.

The Ogawa et al. reference teaches a method of packaging an integrated circuit, figs. 1 and 3, comprising:

providing a lead frame including a plurality of leads 1 and a central opening, the lead frame is made by punching or by etching a plate composed of a copper alloy or an iron alloy, col. 1, lines 13-16, having opposing upper and lower surfaces;

mounting the lead frame1 and an integrated circuit die 4 onto a strip of adhesive tape 2 such that a lower surface of the die contacts the adhesive tape and the die is located in the central opening and the lower surface of the lead frame also contacts the adhesive tape such that the lower surface of the die and the lower surface of the lead frame are substantially co-planar;

electrically connecting bond pads on a top surface of the die to associated lead frame leads, col.5, lines 5-20.

The Ogawa et al. reference does not teach

forming a plastic casing over an upper surface of the die and the upper surface of the lead frame wherein the molded plastic casing comes into contact with the adhesive

tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die; and

removing the adhesive tape after molding the plastic casing to expose the lower surfaces of the die and the leads, whereby exposed portions of the leads form the only external accessible I/O contacts for a resulting integrated circuit package and plastic material fills at least portions of gaps formed between adjacent leads such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die.

The Melton et al. reference discloses a method comprises the steps of:

forming a flat lead frame 22 including a plurality of leads 13, the lead frame having opposing upper and lower surfaces;

mounting the lead frame and an integrated circuit die 12 onto a molding support 38 of flexible polyimide tape having an adhesive coating such that a lower surface of the die contacts the adhesive tape and the die is located in a central opening, and the lower surface of the lead frame also contacts the adhesive tape, "*molding support 38 is formed of a flexible polyimide tape having an adhesive coating for temporarily securing integrated circuit die 12 and lead frame 22 during processing*", col. 2, lines 55-60;

forming a plastic casing 21 *using a dispensing approach* over an upper surface of the die and the upper surface of the lead frame, *the dispensed polymeric precursor is an epoxy resin, col. 3, lines 56, the "resulting polymeric body 14 encapsulates active face 28 of the integrated circuit die 12, the plurality of wire leads 18, inner surface 19 ...*

thereby protecting them from environmental exposure and damage experienced during normal use of microelectronic package 10", col. 4, lines 15-20; and

removing the adhesive tape 38 to expose the lower surfaces of the die and the lead frame *such that "first surface 24, non-active face 32 and outer surface 17 cooperate to form planar surface 37"*, col. 4, lines 22-26 and 66-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the semiconductor package formation of Ogawa et al. with the steps of casing formation and the adhesive tape removing of Melton et al. because the steps of casing and tape removing of Melton et al. would be selected in the manufacturing process to complete the package device as taught by Ogawa et al. and to protect the active face, the wire leads and inner surface of the die as taught by Melton et al. This combination will ensure the adhesive tape holds the die and lead frame in place during the wire bonding operation, the molded plastic casing comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die, and to expose the lower surfaces of the die and the leads, whereby exposed portions of the leads form the only external accessible I/O contacts for a resulting integrated circuit package and plastic material fills at least portions of gaps formed between adjacent leads such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die.

The combination does not disclose the plurality of leads extending radially from a central opening and molding a plastic casing.

The Djennas et al. reference discloses methods for making semiconductor device having no die supporting surface.

In the first embodiment, figs. 4-6, the Djennas et al. reference discloses a method for making semiconductor device having no die supporting surface comprising: forming a flat lead frame including a plurality of leads extending radially from a central opening, "no tie bars, such as shown in FIG. 1 of the prior art", col. 4, lines 10-11, the lead frame having opposing upper and lower surface; the lead frame and an integrated circuit die are mounted onto a supporting work holder; molding a plastic casing over an upper surface of the die and the upper surface of the lead frame; the die includes a plurality of die bond pads so that "the active surface of the semiconductor die 22 is wire bonded to the plurality of conductors 12", col. 4, lines 20-22.

In the third embodiment of figs. 9-10, "the inactive surface of the wire bonded semiconductor die 22 is placed directly on a lower mold platen 92 includes a vacuum line 94 ... aids in the prevention of flash ... a heat sink (not illustrated) can be attached to the exposed inactive surface of the die 22 for enhanced thermal dissipation. In addition to the aforementioned advantages of device 58, another advantage to device 90 is that the total thickness of the device has been decreased because the package body 96 is not a total encapsulation of the semiconductor die 22... a heat sink (not illustrated) can be attached to the exposed inactive surface of the die 22 for enhanced thermal dissipation ... It should be obvious that although device 90 is illustrated to be a

J-lead type of device, other external leads configurations are possible", col. 6, lines 19-50.

The two embodiments do not use removable tape to provide a temporary die supporting surface but use the mold platen or supporting work holder; although, in the sixth embodiment, figs. 18-20, a "removable tape 148 is affixed to the bottom surface of the substrate 100 including the die cavity 102 ... the tape 148 provides a temporary die supporting surface whereupon the semiconductor die 22 is placed", col. 9, lines 6-12; the step of forming the plastic casing comprises molding plastic onto the upper surfaces of the die and the substrate, fig. 19; "the removal of the tape 148 from the bottom of the substrate 100 after the step of molding", col. 9, lines 49-51, whereby exposed portions of the substrate form the only externally accessible I/O contacts for the package, fig. 20. The Djennas et al. reference discloses substantially all of the instant invention and ignores how the conventional lead frame is formed.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the Ogawa/Melton combination with the flat lead frame having leads extending radially from a central opening and the molding step of the Djennas et al. reference as the use of lead frame and the molding step of Djennas et al. would be selected in accordance with the packaging process as taught by the combination. The choice of different lead frames, with radial or non-radial leads and without the die supporting surface, has no impact on the type of lead frame in the assembly of the package in terms of the thickness of the finished device as mentioned

by both Melton and Ogawa et al. references. The molding technique of Djennas et al. would help in "the prevention of flash which may occur as a result of transferring the resin encapsulant into the mold cavity under high pressure" col. 6, lines 28-31.

Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the first and third embodiments formation of Djennas et al. with the lead frame *and the adhesive tape "with sufficient adhesive force" (Ogawa et al.'s col. 2, line 44)"thereby exhibit the anchoring effect against the shear force or peeling force" (Ogawa et al.'s col. 4, lines 1-16)* of Ogawa et al. because the lead frame and adhesive tape of Ogawa would provide the package formation of Djennas et al. with improved reliability (*Ogawa et al.'s* col. 1, line 10).

With this combination, the exposed portions of the leads form the only externally accessible I/O contacts for a resulting integrated circuit package, these only externally accessible I/O contacts at the lower surfaces of the leads would be used to solder the package to the circuit board to electrically connect the package to the circuit board. Further, the Djennas reference teaches "the external portion of the leads can be in any surface mount or through hole configuration... a heat sink may be attached to the inactive surface of the semiconductor die in any of the embodiments provided that the inactive surface is at least partially exposed" (col. 12).

Response to Arguments

5. Applicant's arguments with respect to claim1-10 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant fails to provide evidence that diligence exists, accordingly, it is adequate to use the Melton et al. US patent No. 5,844,315 as prior art against the applicant.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WP
10/20/2005

George Fourson
Primary Examiner